



Innovation Resulting in Cost Reduction

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MIS CHIP CAPACITORS

Tolerance = +/- 10 % on singles; Binary = +/- 20%.

Metallization options:

"A" = AuSn Attach and wire bondable pad

"B" = AuGe attach (backside) and AuSn topside for FET or MMIC Mounting (self bias)

Singles (A)

Part Number	Capacitance (pF)	Standoff Voltage (V)	Chip outline
MP0001	1.0	100	C3
MP0002	2.0	100	C3
MP0003	3.0	100	C3
MP0004	4.0	100	C3
MP0005	5.0	100	C3
MP0010	10.0	100	C3
MP0015	15.0	100	C4
MP0022	22.0	50	C4
MP0033	33.0	50	C4
MP0047	47.0	50	C4
MP0068	68.0	50	C5
MP0100	100.0	50	C6

Binary (A)

Part Number	Capacitance (pF)	Total Capacitance (pF)	Standoff Voltage (V)	Chip outline
MP0402	0.25, 0.50, 1.0, 2.0	3.75	100	C24
MP0404	0.5, 1.0, 2.0, 4.0	7.5	100	C24
MP0408	1.0, 2.0, 4.0, 8.0	15	100	C24
MP0416	2.0, 4.0, 8.0, 16.0	30	100	C24

MMIC/FET Mounting (B)

Part Number	Capacitance (min pF)	Standoff Voltage (V)	Top pad area	Overall Dimensions	Chip Outline
MP0125	125	50	72x72	75x75	C75
MP0150	150	50	108x108	110x110	C110
MP0500	500	50	163x163	165x165	C165